

CLAIM AMENDMENTS

Please **AMEND** claims 46 and 53 as shown in the following claim listing.

Please **CANCEL** claim 57.

A listing of all pending claims with status indicators follows.

1 - 45. (Canceled)

46. (Currently Amended) A liquid crystal display comprising:
a first insulating substrate;
a gate pattern that comprises a gate electrode and a gate line that is disposed on the first insulating substrate;
a gate insulating layer that covers the gate pattern;
a semiconductor layer disposed on the gate insulating layer;
a data pattern that comprises a drain electrode and a source electrode, which are disposed on the semiconductor layer, and a data line that is connected to the drain electrode;
a passivation layer that comprises organic insulating material and has a contact hole that exposes the drain electrode;
a pixel electrode that is connected to the drain electrode through the contact hole;
a second insulating substrate that faces the first insulating substrate;
a black matrix that overlaps the gate line or the data line; and
spacers disposed formed at a region covered by the black matrix between the first insulating substrate and the second insulating substrate.

47. (Previously Presented) The liquid crystal display of claim 46, wherein the dielectric constant of the passivation layer is in a range of about 2.4-4.7.

48. (Previously Presented) The liquid crystal display of claim 46, wherein the passivation layer has a flat surface.

49. (Previously Presented) The liquid crystal display of claim 46, wherein the pixel electrode overlaps at least a portion of the data pattern.

50. (Previously Presented) The liquid crystal display of claim 46, wherein the black matrix is disposed in a groove of the passivation layer.

51. (Previously Presented) The liquid crystal display of claim 46, further comprising an etch stop layer that is disposed between the semiconductor layer and the passivation layer.

52. (Previously Presented) The liquid crystal display of claim 46, wherein the black matrix is formed using photolithography.

53. (Currently Amended) A thin film transistor substrate for a liquid crystal display comprising:

a transparent insulating substrate;

a gate line disposed on the first insulating substrate;

a storage capacitor electrode disposed on the insulating substrate;

a gate insulating layer that covers the gate line and the storage capacitor electrode;
a semiconductor layer disposed on the gate insulating layer;
a data line that crosses the gate line and is disposed on the gate insulating
layer;
a metal pattern that is disposed over the storage capacitor electrode, and is disposed on
the same layer with the data line;
a passivation layer that comprises an organic insulating material and is disposed on the
semiconductor layer and the data line, and has a contact hole that exposes the metal pattern; and
a pixel electrode connected to the metal pattern through the contact hole;
wherein the passivation layer contacts a portion of the semiconductor layer between
source and drain regions thereof.

54. (Previously Presented) The thin film transistor substrate of claim 53, wherein the
dielectric constant of the passivation layer is in a range of about 2.4-4.7.

55. (Previously Presented) The thin film transistor substrate of claim 53, wherein the
passivation layer has a flat surface.

56. (Previously Presented) The thin film transistor substrate of claim 53, wherein the
pixel electrode overlaps at least a portion of the data line.

57. (Cancelled)